

AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method for issuing instructions in a processor having a pipeline, comprising:

(a) providing a loop buffer for holding program loop instructions and a register file having at least three entries for holding speculative and architectural loop control parameters, wherein each entry in the register file comprises a loop top register for holding a loop top address, a loop bottom register for holding a loop bottom address and a loop count register for holding a loop count;

(b) in response to decoding of a first loop setup instruction, marking a first entry in the register file as a current entry and writing in the first entry loop control parameters represented in the first loop setup instruction;

(c) marking the current entry in the register file as an architectural entry in response to the first loop setup instruction being committed in the pipeline;

(d) sending a loop bottom indicator down the pipeline with a loop bottom instruction; and

(e) selecting, in a single loop top selector, only the loop top address of the current entry from the loop top addresses in the register file, comparing, in a single loop top comparator, a current instruction address only with the selected loop top address to determine a loop top match, selecting, in a single loop bottom selector, only the loop bottom address of the current entry from the loop bottom addresses in the register file, and comparing, in a single loop bottom comparator, the current instruction address only with the selected loop bottom address to determine a loop bottom match.

2. (Original) A method as defined in claim 1, further comprising decrementing a loop count in the architectural entry in the register file in response to the loop bottom instruction being committed in the pipeline.

3. (Original) A method as defined in claim 1, further comprising issuing instructions of the program loop according to the loop control parameters in the current entry in the register file.

Do Not Enter